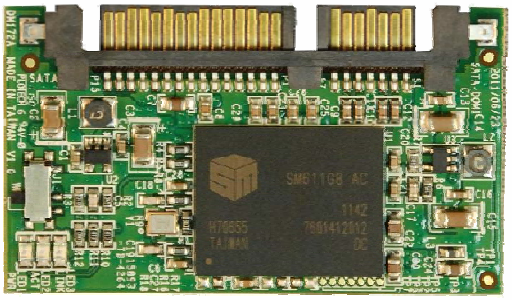
DMP SATA Slim DOM

SDM-SLIM-4G-V
SDM-SLIM-8G-V
SDM-SLIM-16G-V

Datasheet



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Contents

Chapter 1

1. Product Introduction

1.1 Overview

DMP SATA Slim DOM is designed to comply with JEDEC SFF-8156 standard form factor, which is extremely suitable for portable / hand-held devices or thin clients. Moreover, its standard 7+15 pin SATA interface could support most of the platform with standard SATA port. DMP SATA Slim DOM operates under SATA II (3.0Gb/s) protocol with good performance.

DMP SATA Slim DOM is also suitable in industrial field. It effectively reduces the booting time of operation system and the power consumption is less than hard disk drive (HDD). DMP SATA Slim DOM complies with ATA protocol, no additional drivers are required, and the SATA Slim DOM can be configured as a boot device or data storage device.

1.2 Product Features

- Interface: Serial ATA II (3.0Gbps)
- Capacity: 4GB ~ 16GB
- Data transfer rate: (In MB/s, Based on Intel ATOM platform)

SATA Density	Item no	Seq Read	Seq Write	512KB R.R.	512KB R.W.	4KB R.R	4KB R.W.
4GB	SDM-SLIM-4G-V	42.06	6.398	41.36	6.177	8.972	0.64
8GB	SDM-SLIM-8G-V	44.58	6.490	44.19	6.271	10.53	0.61
16GB	SDM-SLIM-16G-V	53.39	11.25	52.86	9.604	11.34	0.62

Table 1: Data transfer rate

- Compact Design: Build-in VCC Power pin (pin 7)
- Access time: 0.3ms
- Error Correction Function
  Built-in ECC corrects up to 15-bit per 512-Byte
- Dimension: 53 x 32 x 4.0 mm

Chapter 2

2.Specifications

2.1 Environmental Specifications

2.1.1 Temperature Range

- Operating Temperature Range
  Standard Grade: 0°C to +70°C

- Storage Temperature Range:
  Standard / Industrial Grade: -40°C to +85°C

2.1.2 Humidity

Relative Humidity: 10-95%, non-condensing

2.1.3 Shock and Vibration

Table 2: Shock / Vibration Testing for DMP SATA Slim DOM

Reliability	Test Conditions
Vibration	7 to 2000 Hz, 20G
Mechanical Shock	Duration: 10ms, 50G

2.2 System Reliability

2.2.1 ECC Technology

High reliability based on the internal error correct code (ECC) function. Built-in ECC corrects up to 8-bit per 512-Byte.

2.2.2 Mean Time between Failures (MTBF)

Table 2 summarizes the MTBF prediction results for various DMP SATA Slim DOM configurations. The analysis is performed using a RAM Commander™ failure rate prediction.

- **Failure Rate:** The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.

- **Mean Time between Failures (MTBF):** A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 3: DMP SATA Slim DOM MTBF

Product	Condition	MTBF (Hours)
DMP SATA Slim DOM	Environment 25°C	> 3,000,000

2.2.3 Transfer Mode

DMP SATA Slim DOM supports the following transfer mode:

- PIO Mode: 0~4
- Multiword DMA: 0~2
- Ultra DMA: 0~6

2.2.4 Data Transfer

The DMP SATA Slim DOM uses a superior DMA technology to transfer data between the host and the NAND flash interface. The DMA technology transfers data at a very high rate in both directions (read and write) and in doing so, effectively decreases the micro processor loading.

2.2.5 SMART Command and Data Security

DMP SATA Slim DOM provides SMART command support that allows users to read spare and bad block information. The users can thus evaluate driver health at run time and receive an early warning before the flash drive lifespan ends. It provides security commands for users to lock and unlock the drive by password or a hardware switch. In additions, customized commands can be utilized to erase blocks for those users who require the highest level of security.

2.3 Power Management

- Prevent SATA corruption
- Automatic Sleep and wake-up mechanism to save power

2.3.1 DC Input Voltage

5V (±5%) single power supply operation

2.3.2 Power Consumption

Table 4: DMP SATA Slim DOM power consumption

Item no	Operation Mode	3.3V(mA) Point A	1.8V(mA) Point B	Total (mW) A*3.3V+B*1.8V	Vcc in Total (mW) Point C
SDM-SLIM-4G-V	Stand by	1	136	248	275
	Read	24	223	481	525
	Write	36	171	427	461
	Slumber	0	88	158	176

Item no	Operation Mode	3.3V(mA) Point A	1.8V(mA) Point B	Total (mW) A*3.3V+B*1.8V	Vcc in Total (mW) Point C
SDM-SLIM-8G-V	Stand by	1	136	248	275
	Read	25	230	497	558
	Write	36	172	428	497
	Slumber	0	88	158	176

Item no	Operation Mode	3.3V(mA) Point A	1.8V(mA) Point B	Total (mW) A*3.3V+B*1.8V	Vcc in Total (mW) Point C
SDM-SLIM-16G-V	Stand by	1	136	248	275
	Read	26	236	511	576
	Write	45	174	462	649
	Slumber	0	88	158	176

Note: The power consumption measurements will vary depending on system and temperature.

2.4 RoHS compliance

DMP SATA Slim DOM is fully compliant with RoHS directive.

Chapter 3

3 Theory of operation

3.1 Overview

Figure 2 shows the operation of DMP SATA Slim DOM from the system level, including the major hardware blocks. As the diagram shown, SATA II controller communicates with SATA II host interface directly. Also SATA II controller supports one flash IC.

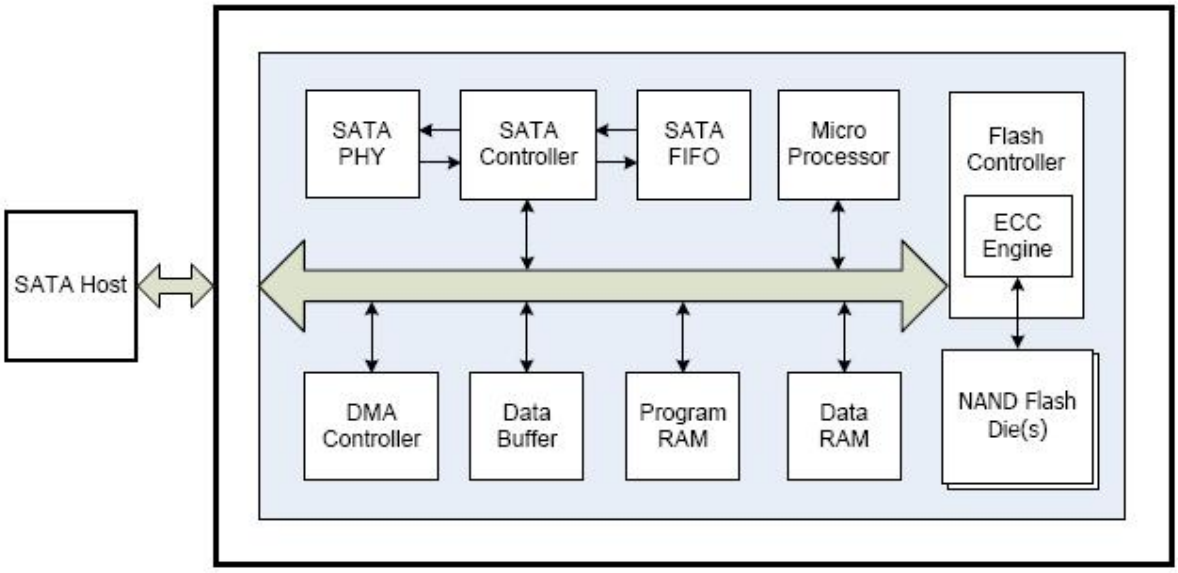

Figure 1: DMP SATA Slim DOM Internal Block Diagram

3.2 SATA II Controller

The SATA II controller is 3.0Gbps, and supports hot-plug. This SATA II controller support four flash IC and communicates with host interface, this SATA II controller can support the flash ICs for 4kbyte per page.

3.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 15 bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

3.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the **erase cycle limit** or **write endurance limit** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.
DMP SATA Slim DOM uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page and block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

3.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the DMP SATA Slim DOM is shipped, or may develop during the life time of the SSD. The Bad Blocks will not exceed more than 6.7% of the total device volume. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The DMP SATA Slim DOM implement Bad Blocks management, Bad Block replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

Chapter 4

4 Installation Requirements

4.1 SATA SLIM DOM Pin Directions

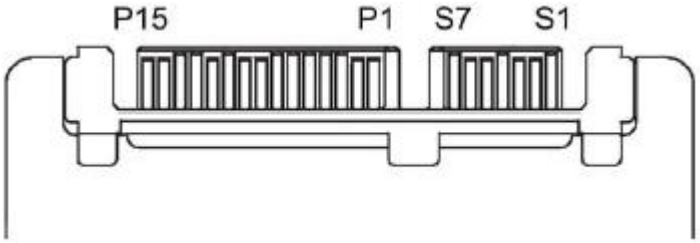

Figure 2: Signal Segment and Power Segment

4.2 Device deriver

No additional device drivers are required. The DMP SATA Slim DOM can be configured as a boot device.

Chapter 5

5 Specifications

5.1 Pin Assignment

DMP SATA Slim DOM is designed within SATA II Interface. Particularly, its built-in power pin enables the device more compactable. Table 4 demonstrates DMP SATA Slim DOM pin assignments.

Table 5: DMP SATA Slim DOM Pin Assignment

Name	Signal	Function
S 1	GND	NA
S 2	A+	Differential signal Pair A
S 3	A-	
S 4	GND	NA
S 5	B-	Differential signal Pair B
S 6	B+	
S 7	GND	NA
Key and Spacing separate signal and power segments		
P1	V33	3.3V Power
P2	V33	3.3V Power
P3	V33	3.3V Power, Pre-charge
P4	GND	NA
P5	GND	NA
P6	GND	NA
P7	V5	5V Power, Pre-Charge
P8	V5	5V Power
P9	V5	5V Power
P10	GND	NA
P11	DAS/DSS	Device Activity Signal / Disable Staggered Spin up
P12	GND	NA
P13	V12	12V Power, Pre-charge
P14	V12	12V Power
P15	V12	12V Power

5.2 Mechanical Dimensions

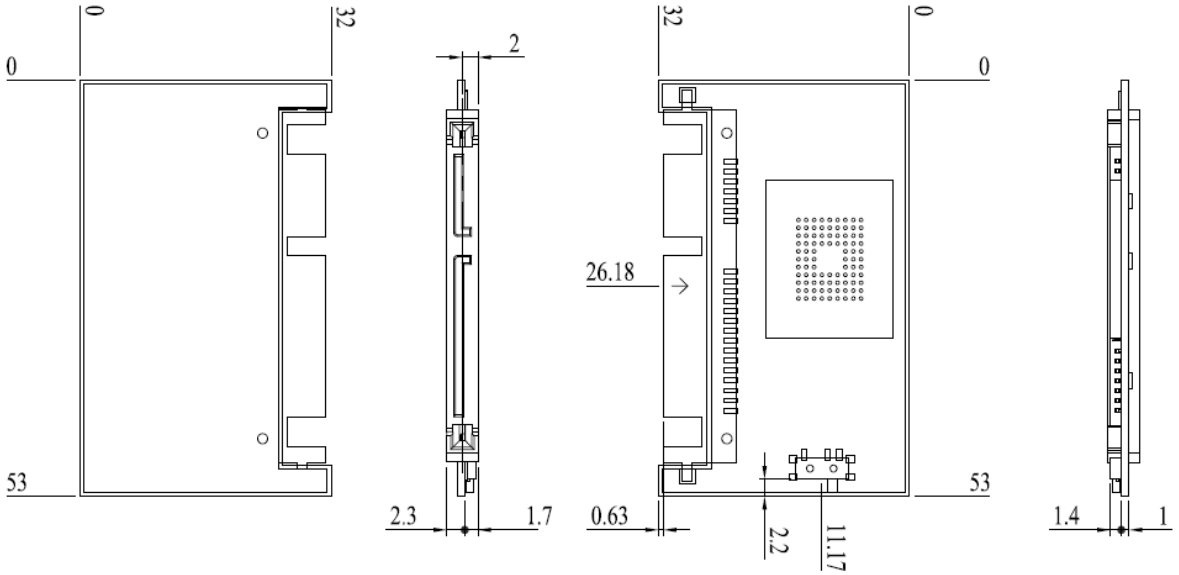

Figure 3: DMP SATA Slim DOM mechanical dimensions

5.3 Performance

A. Burst Speed Rate: 300MB / sec.
B. Data Transfer Rate

SATA Density	Item no	Seq Read	Seq Write	512KB R.R.	512KB R.W.	4KB R.R	4KB R.W.
4GB	SDM-SLIM-4G-V	42.06	6.398	41.36	6.177	8.972	0.64
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Table 1: Data transfer rate

5.4 Seek Time

DMP SATA Slim DOM is not a magnetic rotating design. There is no seek or rotational latency required.

5.5 NAND Flash Memory

DMP SATA Slim DOM uses Multi Level Cell (MLC) NAND and, which are non-volatility, high reliability and high speed memory storage. For MLC, there are four statuses 00, 01, 10 and 11 of one cell. Read or Write data to flash memory for DMP SATA Slim DOM is controlled by micro processor.

Chapter 6

6 Product Ordering information

6.1 Ordering information

SDM-SLIM-4G-V: DMP SATA Slim DOM Pin Vertical with 4GB capacity.
SDM-SLIM-8G-V: DMP SATA Slim DOM Pin Vertical with 8GB capacity.
SDM-SLIM-16G-V: DMP SATA Slim DOM Pin Vertical with 16GB capacity.